current amendment. The attached page is captioned "**Version with markings to show changes made.**"

It is noted that the claim amendments herein are intended solely to correct a typographical error in the description of the present invention as described by claim 21 and to expressly articulate in claims 1 and 21 that the third region is only below the second region and not the first region. These amendments are not for distinguishing over the prior art or the statutory requirements directed to patentability.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Entry is proper under 37 CFR §1.116 since no new claims are added, no new issues are raised, and the present Amendment clarifies the issues for appeal by providing a response to the Examiner's revised rejection wording. Applicant additionally submits that entry is required to permit the Examiner to place the rejections on record into a proper format for the appeal process by providing the rationale either incorrect or missing, as specifically identified below.

Claims 1-27, all of the claims pending in the present Application, stand rejected under 35 USC §103 (a) as being unpatentable over Applicant's Admitted Prior Art, further in view of US Patent 5,945,713 to Voldman.

This rejection is respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

As described and claimed, for example by claim 1, the present invention addresses an

input/output protection device for a semiconductor integrated circuit having a substrate of a first conduction type, an internal circuit, an input/output terminal, electrode wiring, and signal wiring. The protection device includes a first diffusion layer fabricated in a region of the first conduction type of the semiconductor substrate. This layer has a second conduction type opposite the first conduction type and is connected to the input/output terminal.

A second diffusion layer of the second conduction type is held at a predetermined potential. A third diffusion layer of the second conduction type is fabricated at a bottom of the second diffusion layer but not below the first diffusion layer. The third diffusion layer is connected to the second diffusion layer. The first diffusion layer is circularly enclosed with the second and third diffusion layers.

Advantages of the present invention include the feature that an overvoltage at the input terminal causes a rapid turn-on of the lateral NPN transistor comprising the first, second, third, and fourth regions, in conjunction with the substrate. The rapid speed is caused by the blocking action of the third region of carriers, which blocking action allows voltage to quickly build up in the base of the lateral transistor.

II. THE PRIOR ART REJECTION

The Examiner maintains the allegation that the Applicant's Admitted Prior Art, further in view of US Patent 5,945,713 to Voldman, renders the present invention obvious.

However, as pointed out during the personal interview of October 9, 2002, the urged combination of Voldman with the Applicant's Admitted Prior Art has little or no technical foundation, when viewed through the eyes of one of ordinary skill in the art. The Examiner concedes that the Applicant's Admitted Prior Art is deficient to satisfy claim 1 and that the

following changes would be required to the lateral npn transistor shown in Figures 5A/5B showing the Applicant's Admitted Prior Art:

1. The n-type region 105, serving as the emitter for the lateral npn transistor during overvoltage, must be converted from a rectangular region into a guard ring that totally surrounds the collector region 104; and

2. An additional n-type region must be inserted under the circular guard ring, where the additional n-type region extends down to the substrate.

To overcome this deficiency, the Examiner relies upon Figure 8 of Voldman, pointing to diffusion layer 12 as being an n-type (second type) layer fabricated at the bottom of the overlying n+ diffusion layer that is connected to V_{SS}(OCD). The Examiner alleges that one of ordinary skill in the art would be motivated to modify Figures 5A/5B to incorporate the n-well guard ring shown in Voldman to "prevent current flow to the n-channel MOSFET driver circuit, as shown in Voldman".

Applicant again submits that this rejection is totally improper unless the Examiner can point to an n-channel MOSFET driver circuit in Applicant's Admitted Prior Art to which current flow needs to be prevented. Without such driver circuit, the motivation of record is totally meaningless.

As pointed out above, the purpose of the guard ring in the present invention has nothing to do with preventing current from flowing to a driver circuit. Rather, its purpose and one of its advantages over the Applicant's Admitted Prior Art shown in Figure 5A/5B is that it serves to contain charges in the region that serves as the base of the lateral transistor. This containment of charges allows the voltage to very quickly build up, thereby turning on the lateral transistor more quickly.

In total contrast, the n-well 12 of Voldman does not serve a purpose of containing charges. Nor does it provide an improvement in speed of response.

Therefore, the rejection on record is clearly totally improper unless the Examiner provides a reasonable motivation to incorporate the n-well ring guard 12 into the components as they exist in the primary reference (Figure 5A/5B) itself. Here, there is none.

Hence, turning to the clear language of claim 1, there is no teaching or suggestion of "... a third diffusion layer of the second conduction type fabricated at a bottom of the second diffusion layer, the third diffusion layer being connected to the second diffusion layer, ... the first diffusion layer being circularly enclosed with the second and third diffusion layers." Similar language is in claim 21.

Additionally, to clarify the present invention more explicitly, Applicant has amended claims 1 and 21 to expressly articulate that the third diffusion region is below only the second diffusion region but not below the first diffusion region.

In Voldman, n-well 12 is clearly provided beneath every n+ diffusion layer, including the one connected to the input/output terminal 10.

In contrast, in the present invention, the third diffusion layer 7, 7a is not formed at the bottom of the first diffusion layer 4, which is connected to the input/output terminal. Therefore, an avalanche breakdown occurs at the junction region between the semiconductor substrate of the first conduction type or the fourth diffusion layer 2a and the first diffusion layer 4.

The breakdown current caused by this avalanche breakdown will flow in a longitudinal direction because of the diffusion layer 3, and further flow into the lead (extraction) diffusion layer 6 through the substrate. In this way, the path for the breakdown current becomes

longer, and there will be a larger voltage drop. Consequently, the electric potential of the semiconductor substrate or the fourth diffusion layer 2a will rise quickly. Therefore, the present invention can operate as a high speed lateral type bipolar transistor having the first diffusion layer 4 as a collector, and the second diffusion layer 5 and the third diffusion layer 7 as an emitter.

Hence, turning to the clear language of claims 1 and 21, there is no teaching or suggestion of "... said third diffusion layer being fabricated at other than a bottom of said first diffusion layer ...."

Additionally, prior to imminent appeal, Applicant respectfully request that the Examiner place the existing remaining rejections into proper condition for appeal, as follows.

- Relative to the rejection for claims 3 and 22, Applicants request that the Examiner provide an explanation why it would be desirable to construct a typical p-well 102 shown in Figure 5B with the monotonously-decreasing concentration such as shown in Figure 2. A typical n-well would not have such monotonous concentration.

- Regarding the rejection for claims 4 and 13, the Examiner is requested to provide a definition of "optimum" that becomes meaningful in the context of incorporating guard ring 12 into Figure 5B. That is, it is obvious that Figure 8 of Voldman does not even contain a p-well corresponding to p-well 102 of Figure 5B. This missing layer is because the n-well guard ring 12 in Voldman does not have a charge containment function. If the Examiner's motivation to combine Voldman into Figure 5B were reasonable ("to prevent current flow to the n-channel MOSFET driver circuit, as shown in Voldman"), the "optimum" condition of having the guard as extending through p-well layer 102 in Figure 5B necessarily means that the mysterious "n-channel MOSFET driver circuit" that the Examiner relies upon must necessarily be located

somewhere outside the components shown in Figure 5B. The Examiner is requested to point out this mysterious "n-channel MOSFET driver circuit" in Figure 5B.

- Relative to the rejection for claims 7-10 and 24, the Examiner is requested to identify for the Appeal panel the labels for the gate structure that is alleged to be present in Figure 5B.

- Relative to the rejection for claim 8, the Examiner is understood as taking Official Notice that circular-shaped gate structures are common in the art. Applicant respectfully requests that the Examiner provide a reasonable reference, properly combinable withVoldman and Figure 5A/5B, for such allegation.

- Relative to the rejection for claims 9 and 10, the Examiner is understood as taking Official Notice and requests that the Examiner provide a reasonable reference.

- Relative to the rejection for claim 21, the Examiner is requested to provide a reasonable rejection in which the fourth region is enclosed by the substrate and the first, second, and third regions. That is, even if the n-well guard ring 12 of Voldman were incorporated into Figure 5A/5B, it would fail to suggest a fourth region unless the guardring extends down through layer 102 to reach the substrate 101.

Clearly, until a proper rejection under 35 USC §103(a) is placed on the record that properly addresses the deficiencies identified above, for all of the reasons above, the claimed invention is fully patentable over the Applicant's Admitted Prior Art.

Further, the other prior art of record has been reviewed, but it too, even in combination with Applicant's Admitted Prior Art and Voldman, fails to teach or suggest the claimed invention.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-27, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 3/7/03

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claims 1 and 21 have been amended, as follows:

1. (Amended) An input/output protection device for a semiconductor integrated circuit having a substrate of a first conduction type, an internal circuit, an input/output terminal, electrode wiring, and signal wiring, said protection device comprising:

a first diffusion layer fabricated in a region of the first conduction type of the semiconductor substrate, the layer having a second conduction type opposite the first conduction type and being connected to the input/output terminal;

a second diffusion layer of the second conduction type being held at a predetermined potential; and

a third diffusion layer of the second conduction type fabricated at a bottom of the second diffusion layer, the third diffusion layer being connected to the second diffusion layer, said third diffusion layer being fabricated at other than a bottom of said first diffusion layer,

the first diffusion layer being circularly enclosed with the second and third diffusion layers.

21. (Amended) An input/output protection device for a semiconductor integrated circuit, said protection device comprising:

a substrate having a first conduction type;

a first region having a second conduction type opposite said first conduction type, said first region connected to an input/output terminal;

a second region enclosing said first region, said second region having said second conduction type, said first region and said second region being electrically separated;

a third region formed adjacent said second region, said third region having said second conduction type, said third region being formed below said second region at other than a bottom of said first region; and

a fourth region surrounded by said substrate and said first, second, and third regions, said fourth region having said [second] first conduction type.